I claim:

1. In the fabrication of microelectronic devices on silicon semiconductor wafers, where delicate microcircuits are formed on the front face of a flat silicon wafer having a diameter of at least 200 mm by more than 200 steps including many layering, patterning and doping operations and at least 30 wet processing steps, characterized in that each semiconductor wafer is electrically charged from a direct current source during wet processing steps to provide an effective field intensity.

2. A process according to claim 1 characterized in that the field intensity at the wafer surface is sufficient to dislodge and remove sub 0.1 micron particles.

3. A process according to claim 1 wherein a wafer is charged to a voltage of from about 2 to about 60 volts during wet processing operations.

4. A process according to claim 1 wherein a wet processing operation includes chemical mechanical polishing with colloidal-size abrasive particles and subsequent chemical cleaning of each wafer to remove such particles while the wafer is charged to a voltage sufficient to dislodge and repel colloidal-size particles.

5. A wafer cleaning process according to claim 1 wherein a wet processing operation includes treatment of each wafer with a dilute high-purity acid solution while the wafer surface is electrically charged.

6. A process according to claim 1 wherein the wet processing operation includes treatment of each wafer by a non polar compound, such as isopropyl alcohol, 1-methoxy-2-propanol or di-acetone alcohol, before drying the wafer.

3 7. A process according to claim 1 wherein particulate contaminants are removed and substantially eliminated from a wafer by charging the wafer with a negative voltage of from about 2 to about 60 volts while providing a field intensity of at least 0.02 volts/mm at the wafer surface sufficient to dislodge, remove and repel substantially all of the harmful sub 0.1-micron particles.

6 ~~8.~~ A wet cleaning process wherein a semiconductor wafer is cleaned by thorough rinsing in DI water characterized in that the wafer is charged during rinsing to a voltage of at least 100 volts in such manner that colloidal-size and submicron killer particles bonded to the front face of the wafer containing the delicate microcircuits are effectively removed or eliminated.

7 ~~9.~~ A process for economical wet cleaning of semiconductor wafers during the fabrication of microelectronic devices wherein a single flat wafer is mounted in a fixed position in a narrow shaped receptacle having a flat wall portion parallel to the front face of the wafer and spaced therefrom a short distance, preferably less than 5 mm, and wherein a sequence of several wet cleaning operations is performed on said wafer while it is held in the desired position in said receptacle.

10. A process according to claim 9 wherein the semiconductor wafer is subjected to a series of RCA wet cleaning operations, and megasonic energy is directed generally to the front of said wafer during such operations.

11. A process according to claim 9 wherein an SC-1 cleaning operation is employed using a solution of water, hydrogen peroxide, and ammonium hydroxide including from about 10 to abut 30 percent by weight of an alcohol, such as ethyl alcohol or isopropyl alcohol.

12. A process according to claim 9 wherein at least one face of the semiconductor wafer is charged to a limited but effective voltage, such as 2 to 60 volts, during a wet cleaning operation in said receptacle.

13. A process according to claim 9 wherein a flat electrode with a diameter or width comparable to or larger than that of the semiconductor is provided at the outer face of the glass receptacle to induce the desired electrical charge at the wafer surface during wet cleaning.

14. A process according to claim 3 wherein the front face of one thin plate or wafer containing the delicate microelectronic devices is subjected to a series of wet cleaning steps while that plate is mounted in a fixed position in the internal cavity of a flattened quartz glass receptacle.

15. Apparatus of the character described for wet cleaning of wafers during the fabrication of microelectronic devices comprising a shaped receptacle having a cavity for

receiving at least one semiconductor wafer, means for admitting a liquid to said cavity, and means for charging said wafer with a limited voltage effective to facilitate removal of submicron particulates.

16. Apparatus according to claim 15 for wet cleaning of wafers during the fabrication of microelectronic devices comprising a shaped receptacle with a narrow cavity of a size to receive a single flat wafer, said receptacle having a flat wall portion parallel to the wafer and spaced from the wafer a distance of from about 1 to about 5 mm to cause uniform flow over the entire face of the wafer.

17. Apparatus according to claim 16 wherein a process wafer is mounted in said cavity and exterior means are provided to induce an electric charge of at least 2 volts in said wafer during wet cleaning.

18. A process ~~of the character described~~ for fabrication of microelectronic devices on silicon wafers wherein microcircuits are formed on the front face of a wafer by a plurality of layering, patterning, doping and heating operations and the wafer is wetted and repeatedly subjected to cleaning, rinsing and drying operations to remove contaminants, characterized in that said front face of the process wafer is artificially charged during wet processing with a negative voltage of at least 2 volts sufficient to facilitate removal of sub 0.1 micron contaminant particles bonded to the wafer surface during the wet cleaning operations.

19. A process according to claim 18 wherein the front face of the process wafer is subjected to wet CMP polishing with colloidal silica or alumina particles having an average particle size of from 0.01 to 0.03 microns and is thereafter subjected to chemical cleaning and DI rinsing operations while said front face is negatively charged to a voltage sufficient to cause efficient or substantially complete removal of sub 0.05-micron contaminant particles bonded to the wafer surface.

20. A process according to claim 1 for fabrication of microchips having a minimum line width or circuit image size less than 0.15 microns wherein the front face of each wafer is subjected to the wet CMP polishing with colloidal silica or alumina particles and is thereafter subjected to a wet cleaning operation for 0.5 to 5 minutes while said front face is negatively charged to a substantial voltage, such as 10 to 40 volts or more, sufficient to remove colloidal or sub 0.05 - micron contaminant particles, the voltage and rate of large of the wafer surface being applied or controlled during said wet cleaning operation in such manner as to minimize or limit damage or alteration of the delicate microcircuitry.

21. In a process of the character described for forming delicate microcircuits on the front face of a semiconductor wafer wherein the wafer is subjected to a large number of layering, patterning and doping operations and many wet processing steps to remove organic, metallic and particulate contaminants, the improvement in which the front face of the wafer is provided with a limited electric charge of at least 2 volts during wet processing steps insufficient to degrade the microcircuits, the charge being sufficient to provide a field intensity at said front face effective to dislodge and remove sub 0.1-micron particles bonded at the wafer surface.

22. A process according to claim 20 wherein said field intensity is at least 0.02 volts/mm and sufficient to provide efficient removal of colloidal-size particles.

23. A process according to claim 22 wherein the front face of the wafer is charged to a voltage of from about 1 to about 60 volts.

24. A process according to claim 23 wherein a single silicon wafer with a diameter of at least about 200 mm having a front face with microcircuits having a feature size or line width less than 0.18 micron is wetted and cleaned by charging said front face to a voltage of from 2 to 60 volts, thereby causing colloidal-size particles to be dislodged, released and removed.

25. A process according to claim 24 wherein the front face of the wafer is charged to a field intensity of at least 0.02 volts/mm during washing of the wafer in a highly dilute alkaline solution.

26. In the manufacture of advanced microchips, a process for forming delicate microcircuits on the flat face of a semiconductor wafer in which the wafer is subjected to a large number of layering, patterning and doping operations and many wet cleaning steps with acid and alkaline solutions and pure water to remove intolerable contaminants, characterized in that the wafer face containing said microcircuits is electrically charged to a limited voltage of at least 2 volts to provide an effective field intensity that causes sub 0.1 micron particles bonded at the wafer face to be released and removed.

27. A process according to claim 26 wherein said wafer face is negatively charged to a voltage of from 2 to 60 volts sufficient to cause efficient removal of harmful particles with a particle size of from 0.01 to 0.1 micron.

28. A process according to claim 26 wherein said wafer face is provided with a limited electric charge of at least 10 volts during most of said wet cleaning steps to minimize particulate contamination.

29. In the manufacture of advanced microchips from flat semiconductor wafers having delicate microcircuits formed on one face, an RCA-type wet cleaning process wherein a single wafer is treated in an aqueous alkaline solution containing hydrogen peroxide and thereafter treated in an acidic solution, rinsed in pure water and dried, characterized in that the wafer surface containing said delicate microcircuits is electrically charged during the wet cleaning process to cause effective removal of sub 0.05-micron particles that are strongly bonded to the wafer face.

29.

30. A wafer cleaning process according to claim 29 wherein megasonic energy is employed to assist in the removal of the contaminating particles during the treatment in the alkaline solution and said wafer surface is charged to a negative voltage of from 2 to 60 volts during the cleaning and rinsing steps.

Add B'7